

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Currently Amended) A semiconductor device, comprising:

an insulated gate field effect transistor including

5 a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type;

a second source/drain area of the second conductivity type formed in the semiconductor area; and

10 a gate electrode structure formed on a gate insulating film on a channel area disposed between the first source/drain area and the second source/drain area, the gate insulating film includes a first gate insulating film formed on a first channel area portion and a second gate insulating film formed on a second channel area portion, the gate electrode structure including a first gate electrode and a second gate electrode electrically connected through a third gate electrode; wherein

15 a second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area when viewed from the gate structure and a thickness of the first gate insulating film is different from
20 a thickness of the second gate insulating film.

2. (Original) The semiconductor device according to claim 1, wherein:

a first type impurity concentration distribution in the first channel area portion is different from the first type impurity concentration distribution in the second channel area portion.

25 3. (Currently Amended) The semiconductor device according to claim 1, wherein:

the first gate electrode and the second gate electrode are formed in a side wall configuration with the first gate electrode and the second gate electrode being generally parallel with one another in a direction perpendicular to the gate insulating film.

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4. (Cancelled) The semiconductor device according to claim 1, wherein:

the first gate electrode and second gate electrode are electrically connected through a third gate electrode.

5 5. (Original) The semiconductor device according to claim 1, wherein:

an insulating film is formed between the first gate electrode and the second gate electrode.

6. (Previously Presented) The semiconductor device according to claim 1, wherein:

the first channel area portion is adjacent to the first source/drain area and
10 the second channel area portion is adjacent to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area and the first gate insulating film is thicker than the second gate insulating film.

15 7. (Original) The semiconductor device according to claim 1, further including:

a capacitor electrically connected to the first source/drain area; and
a bit line electrically connected to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area.

20 8. (Original) The semiconductor device according to claim 7, wherein:

the second source/drain area provides a common source/drain area for a pair of memory cells.

9. (Withdrawn) A semiconductor device, comprising:

an insulated gate field effect transistor including
25 a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type;
a second source/drain area of the second conductivity type formed in the semiconductor area; and

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a gate electrode formed on a gate insulating film on a channel area disposed between the first source/drain area and the second source/drain area, the channel area including a first channel area and a second channel area, wherein

5 a second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area and a first type impurity concentration distribution of the first channel area is different from the first type impurity concentration distribution of the second channel area.

10 10. (Withdrawn) The semiconductor device according to claim 9, wherein:

the gate insulating film includes a first gate insulating film formed on the first channel area and a second gate insulating film formed on the second channel area and a thickness of the first gate insulating film is different from a thickness of the second gate insulating film; and

15 the gate electrode includes a first gate electrode and a second gate electrode and the first gate electrode is formed on the first gate insulating film and the second gate electrode is formed on the second gate insulating film.

11. (Withdrawn) The semiconductor device of claim 10, wherein:

20 the first gate electrode and the second gate electrode are formed in a side wall configuration.

12. (Withdrawn) The semiconductor device of claim 10, wherein:

the first gate electrode and second gate electrode are electrically connected through a third gate electrode.

13. (Withdrawn) The semiconductor device of claim 10, wherein:

25 an insulating film is formed between the first gate electrode and the second gate electrode.

14. (Withdrawn) The semiconductor device of claim 9, further including:

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the first channel area is adjacent to the first source/drain area and the second channel area is adjacent to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area and the first
5 type impurity concentration in the first channel area is lower than the first type impurity concentration in the second channel area.

15. **(Withdrawn)** The semiconductor device of claim 9, further including:

a capacitor electrically connected to the first source/drain area; and
a bit line electrically connected to the second source/drain area wherein the
10 second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area.

Claims 16 to 20 (Cancelled)

21. **(Withdrawn)** A semiconductor device, comprising:

15 an insulated gate field effect transistor including
a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type;
a second source/drain area of the second conductivity type formed in the semiconductor area; and
20 a gate electrode formed on a gate insulating film on a channel area disposed between the first source/drain area and the second source/drain area, the channel area including a first channel area adjacent to the first source/drain area and a second channel area adjacent to the second source/drain area, wherein
a second type impurity concentration distribution in the first source/drain
25 area is higher than the second type impurity concentration distribution in the second source/drain area and a first type impurity concentration distribution of the first channel area is lower than the first type impurity concentration distribution of the second channel area.

30 22. **(Withdrawn)** The semiconductor device of claim 21, wherein:

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the first source/drain area and the second source/drain area are lightly doped drain configurations.

23. **(Withdrawn)** The semiconductor device of claim 21, wherein:

5 the second type impurity concentration distribution in the first source/drain area is more shallow than the second type impurity concentration distribution in the second source/drain area.

24. **(Withdrawn)** The semiconductor device of claim 21, wherein:

10 the gate insulating film includes a first gate insulating film formed on the first channel area and a second gate insulating film formed on the second channel area and a thickness of the first gate insulating film is greater than a thickness of the second gate insulating film; and

15 the gate electrode includes a first gate electrode and a second gate electrode and the first gate electrode is formed on the first gate insulating film and the second gate electrode is formed on the second gate insulating film.

25. **(Withdrawn)** The semiconductor device of claim 21, wherein:

the semiconductor device is a semiconductor memory device.

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